In step **150**, the via **130** is formed from the bottom face **9** of the substrate. Step **150** is, for example, identical to step **142** except that the via is hollowed out from the face **9**.

In step **152**, the insulating layer **114** and the coating **132** are deposited. In some practices, step **152** is carried out in the same way as step **144**, but in the via **130**.

In step **154**, only the bottom of the via **132** is etched until the end **62** of the extension **52** is bared. For example, this step is carried out using an RIE etching.

In step **156**, if necessary, a bond coat is deposited. This step **156** is, for example, carried out like step **146**.

In step **158**, the conductor **112** is deposited. In some practices, this step is carried out like step **148**.

Finally, in step **160**, the track **122** is shaped. In some practices, this step is carried out like step **149**.

FIG. **14** represents an integrated circuit **170**. This integrated circuit **170** comprises two electronic chips **172** and **173** stacked one above the other and housed inside one and the same package equipped with connecting leads or pads.

More specifically, the integrated circuit **170** comprises a substrate **174** extending essentially in a horizontal plane. The substrate **174** comprises a top face **176** and a bottom face **178** situated on the opposite side. The thickness of the substrate **174** is, for example, the same as the thickness of the substrate **6**.

In the illustrated embodiment, the substrate **174** is a multilayer substrate produced by the assembly, one on top of the other with no degree of freedom, of a plurality of layers in the Z direction. For example, the different layers are assembled one on top of the other using fusible balls such as balls **180** produced in a brazing alloy. Typically, the brazing alloy comprises tin. In FIG. **14**, the balls **180** are not represented to scale. Thus, the space between the different layers forming the substrate **174** is exaggerated in this figure.

To simplify FIG. **14**, only two horizontal layers **188** and **190** are represented. The top face of the layer **188** corresponds to the face **176**. A bottom face **192** of this layer **188** is turned towards a top face **193** of the layer **190**. These faces **192** and **193** are assembled one on top of the other with no degree of freedom. Typically, electronic components are produced on the face **193** to form the chip **173**. Similarly, the electronic components are implanted in the face **176** or in the face **192** to form the electronic chip **172**. In some embodiments, the layers **188** and **190** are made of silicon.

The integrated circuit **170** also comprises a temperature probe **194** that makes it possible to measure the temperature inside the substrate **6** at the assembly interface between the layers **188** and **190**. This probe **194** comprises two electrical conductors **196** and **198**. It is electrically insulated from the substrate **174**. The conductors **196** and **198** are electrically insulated from one another except at an electrical junction **200**.

To simplify FIG. **14** and the following figures, the insulating layers and the insulating coatings are not represented.

In this embodiment, the ends of the conductors **196** and **198** that form the junction **200** are produced in the same materials as, respectively, the conductors **14** and **18**.

The conductor **196** comprises: an electrical track **206** produced on the face **192**, a bump contact **208** produced on the outer face **176** of the substrate **174**, and an extension **210** electrically connecting the track **206** to the bump contact **208**.

The bump contact **208** fulfills the same function as the bump contact **30**. To this end, for example, it is configured in the same way.

The extension **210** passes vertically right through the layer **188** to emerge, on one side, under the bump contact **208** and, on the opposite side, under the track **206**. Typically, the extension **210** is a via, also better known by the acronym TSV ("Through Silicon Via").

The track **206** extends horizontally between the extension **210** and a distal end **212**. The distal end **212** is in mechanical contact directly with a corresponding distal end **214** of the electrical conductor **198** to form the junction **200**.

In this embodiment, the conductor **198** and the conductor **196** are symmetrical relative to a vertical plane passing through the junction **200**, except at the end **214**.

In FIG. **14**, the bump contact, the extension, and the electrical track of the electrical conductor **198** bear, respectively, the numerical references **216**, **218** and **220**.

The end **214** overlaps the end **212** in the Z direction. Thus, it covers the end **212**. The overlapping surface area is typically greater than 10 $\mu m^2$ and, preferably, greater than 100 $\mu m^2$.

The operation of the temperature probe **194** is deducted from the operation of the probe **12**.

FIG. **15** represents a method for fabricating the integrated circuit **170**. This fabrication method is identical to that of FIG. **3**, except that step **72** is replaced by step **230**.

Step **230** begins with step **232** for producing through vias in the position of the future extensions **210** and **218**. In some practices, step **232** is carried out in the same way as step **74**.

In step **234**, if necessary, an insulating layer is deposited on the face **176** and on the inner walls of the vias. For example, this step is carried out like step **76**.

In step **236**, if necessary, a bond coat is deposited. In some practices, this step is carried out in the same way as step **78**.

In step **238**, the conductive material used to form the conductor **196** is deposited and then shaped by photolithography and etching to obtain the bump contact **208** and the extension **210**. In some practices, this step is carried out in the same way as step **82**.

In step **240**, the conductive material used to form the electrical conductor **198** is deposited, then shaped by photolithography and etching to form the bump contact **216** and the extension **218**. In some practices, this step is carried out in the same way as step **88**.

In step **242**, an insulating layer is deposited on the face **192**. In some practices, this step **242** is carried out in the same way as step **234**.

In step **244**, the conductive material of the track **206** is deposited then shaped by photolithography and etching so as to obtain the track **206**. In some practices, this step is carried out in the same way as step **238**.

In step **246**, the conductive material of the track **220** is deposited then shaped to obtain this track **220**. This step is carried out in the same way as step **244**.

Finally, in step **250**, the layer **188** is assembled on the layer **190** to form the substrate **174** containing the junction **200** buried inside this substrate at the interface between these layers.

FIG. **16** represents an integrated circuit **260**. This integrated circuit **260** is identical to the integrated circuit **170** except that the electrical conductors **196** and **198** are replaced, respectively, by electrical conductors **262** and **264**.

The electrical conductor **262** is identical to the conductor **196** except that the bump contact **208** and the track **206** are replaced, respectively, by a lateral bump contact **266** and a track **268**. Furthermore, the extension **210** is omitted. The bump contact **266** is produced on a vertical side of the layer **188**.

The track **268** is identical to the track **206** except that it is extended in the horizontal plane to emerge under the bump contact **266**.